**9. 3bit Controlled up / down synchronous counter with preset & clear.**

**AIM : -S**imulation of **3 bit Connter** using Behavioral modeling.

**OBJECTIVE:** T**o** learn behavioral modeling style. Its uses and different types of declarations with some different types of circuits. Structure of VHDL program is well discussed with this modeling style

**THEORY :-**

**Behavioral style:-**

Highest level of abstraction supported in VHDL is called the behavior level of abstraction. In it we have for loop, while loop, If then else, case &variable assignment. The statements are enclosed in a PROCESS block, & are executed sequentially.

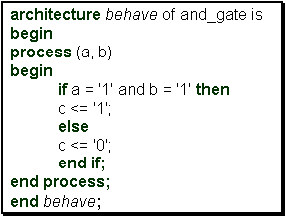
In it circuit is described in terms of its operation overtime.

In behavioral description, the concept of time may be expressed precisely, with actual delays between related events (such as the propagation delays within gates & on wires.) or it may be simply an ordering of operation that are expressed sequentially (such as in a functional description of a F/F).

A behavioral design method defines a circuit in terms of text language rather than a schematic of interconnected symbols.

Behavioral design is a technology independent, text based design that incorporates high level functionality & high level information flow.

**Structure of Behavioral modeling:**

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**Functional block diagram of 3 bit controlled up / down synchronous counter with preset & clear:**

**Function table of 3 bit controlled up / down synchronous counter with preset & clear:**

**Design steps:**

* Click on Xilinx ISE 9.2i.
* Create New project from file menu. Ensure top level source is HDL.
* Select family of devices (usually spartan2E or 3)
* Ensure preferred language is VHDL.
* Click new source which shows you project details, device details
* and Synthesis and simulator tools.
* After finishing project create new source by right clicking in project name with VHDL module.
* Complete ports name, directions and bus. Ensure architecture name is behavioral.
* After that we will get design summary and detailed reports.
* Close design summary.
* Create your code with given modeling style.
* Go to process window and synthesis to check if any error is there in code. Check syntax and view RTL schematic. Create new source to simulate the code
* Right click on source name and create test bench waveform with proper name. Ensure the project is same.
* Click on combinational circuit in initial timing wizard.
* Select test bench wave in source window. Apply inputs to wave diagram. Ensure you are in behavioral simulation.

Go to process box. Click on Xilinx ISE simulator and simulate the model.

**RTL Schematic:**

**Timing Diagram**

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**INPUT:**

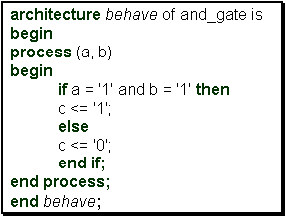
* Clock, Preset, Clear

**OUTPUT:**

* Three output lines,

**FAQ’s:**

1. Explain the structure of behavioral modeling?

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1. What are the differences between behavioral and structural modeling?

**Ans:** Behavioral descriptionof a circuit is the highest level of abstraction in VHDL. Here, the circuit is described in terms of it operation with respect to time. All operations are in one level of code. The operations are described in a way that the designer of a sequential circuit infers a register

Structural description***,*** on the other hand, is a circuit description in terms of its components. it can either create a low level description, much like a hierarchy in a block diagram. Whenever you see a *component* instantiated in a code, that code employs structural description of the circuit. The components are connected in the form of a *netlist*. This is for better manageability and reusability

1. What are the differences between behavioral and data flow modeling?

**Ans:** Behavioral – describes how the output is derived from the inputs using structured statements.

Dataflow – describes how the data flows from the inputs to the output most often

using NOT, AND and OR operations

1. What do you mean by *process* statement?

**Ans:** The process statement begins with the PROCESS keyword, followed by a parenthesized list of signals, called the sensitivity list. It operates on selected and conditional statements.

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1. Explain syntax of *process* statement?

**Ans: BEGIN**

**Process( sensitivity list)**

**;**

**;**

**END process;**

**PRACTICE ASSIGNMENTS:**

1. Implement 3 bit asynchronous up counter using behavioral modeling.

2. Implement 3 bit asynchronous down counter using behavioral modeling.

3. Implement 3 bit synchronous down counter using behavioral modeling.